ABSTRACT OF THE DISCLOSURE

A non-volatile semiconductor memory device includes: a memory cell array having NAND strings arranged therein, each NAND string having a plurality of electrically rewritable and non-volatile memory transistors connected in series; and an erase/write/read control circuit configured to perform erasing, writing and reading of the memory cell array, wherein at least one memory transistor within each NAND string of the memory cell array is controlled as a block separation transistor for dividing the memory cell array into a plurality of blocks each serving as a unit of data erasure.